PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04J 3/07, H04L 25/02, G06F 5/06 — A1

(11) International Publication Number: WO 97/17777

(43) International Publication Date: 15 May 1997 (15.05.97)

(21) International Application Number: PCT/SE96/01415

(22) International Filing Date: 4 November 1996 (04.11.96)

(30) Priority Data:
9503908-7 6 November 1995 (06.11.95) SE

(71) Applicant *(for all designated States except US)*: TELEFONAKTIEBOLAGET LM ERICSSON (publ) [SE/SE]; S-126 25 Stockholm (SE).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: NYBERG, Nils, Henrik [SE/SE]; Kubikenborgsvägen 5, S-122 41 Enskede (SE).

(74) Agent: LINDBLOM, Erik, J.; Flotthamn, S-150 23 Enhörna (SE).

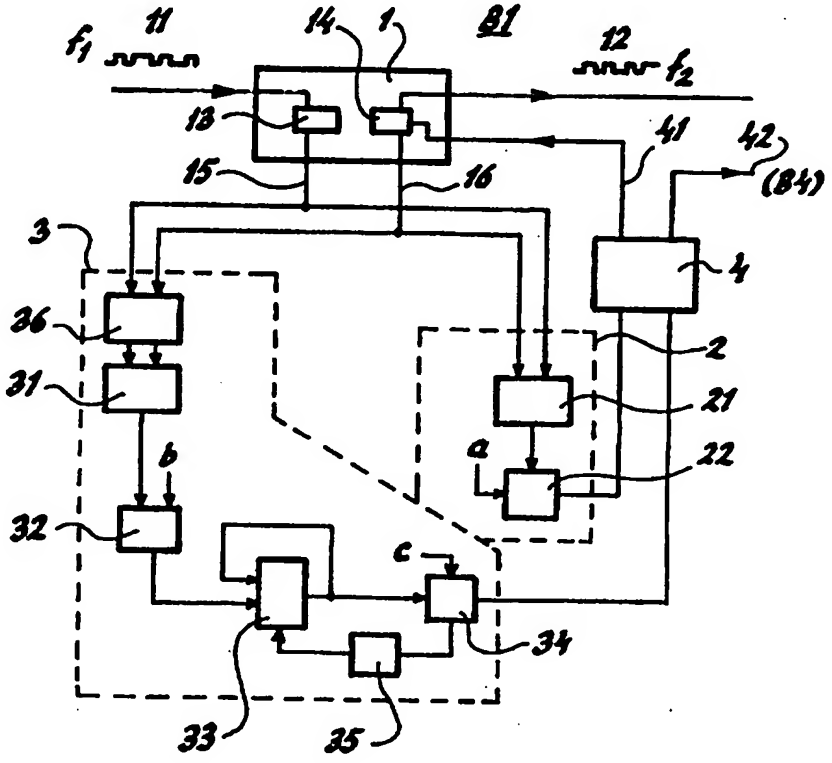
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: A SYSTEM RELATED TO A TRANSMISSION BUFFER

(57) Abstract

The present invention relates to a system for checking and adjusting a transmission buffer (1), wherein a bit stream (11) incoming to the transmission buffer (1) has a first transmission frequency (f_1) or bit rate, and wherein a bit stream (12) outgoing fromthe transmission buffer (1) has a second transmission frequency (f_2) or bit rate. A write-related pointer (15) is given a value which corresponds to a bit position into which a writing unit (13) writes from the incoming bit stream (11) into the transmission buffer (1), and a read-related pointer (16) is given a value which corresponds to a bit position from which a reading unit (14) reads from the transmission buffer (1) into the outgoing bit stream (12). A checking and adjusting means includes a proportional part (2), and integrating part (3) and an adjusting part (5) and functions to check and adjust the bit distance between the writing unit (13) and the reading unit (14). The proportional part (2) operates at a first clock frequency and the integrating part (3) operates at a second clock frequency, wherein the second clock frequency is allocated a lower value than the first clock frequency.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	GB	United Kingdom	MW	Malawi
AT	Austria	GE	Georgia	MX	Mexico
AU	Australia	GN	Guinea	NE	Niger
BB	Barbados	GR	Greece	NL	Netherlands
BE	Belgium	HU	Hungary	NO	Norway
BF	Burkina Faso	IE	Ireland	NZ	New Zealand
BG	Bulgaria	IT	Italy	PL	Poland
BJ	Benin	JP	Japan	PT	Portugal
BR	Brazil	KE	Kenya	RO	Romania
BY	Belarus	KG	Kyrgystan	RU	Russian Federation
CA	Canada	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic			SE	Sweden
CG	Congo	KR	Republic of Korea	SG	Singapore
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LI	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LR	Liberia	SZ	Swaziland
CS	Czechoslovakia	LT	Lithuania	TD	Chad
CZ	Czech Republic	LU	Luxembourg	TG	Togo
DE	Germany	LV	Latvia	TJ	Tajikistan
DK	Denmark	MC	Monaco	TT	Trinidad and Tobago
EE	Estonia	MD	Republic of Moldova	UA	Ukraine
ES	Spain	MG	Madagascar	UG	Uganda
FI	Finland	ML	Mali	US	United States of America
FR	France	MN	Mongolia	UZ	Uzbekistan
GA	Gabon	MR	Mauritania	VN	Viet Nam

TITLE OF THE INVENTION:
A System related to a Transmission Buffer.

FIELD OF INVENTION

The present invention relates to a system for checking and adjusting a transmission buffer in a transmission system with digital information carrying signals, wherein a bit stream incoming to the transmission buffer has a first transmission frequency or bit rate, and wherein a bit stream outgoing from the transmission buffer has a second transmission frequency or bit rate.

The transmission buffer is adapted so that information allocated to each of the bits of the incoming bit stream can be written into the buffer via a writing unit, whereafter the same information can be read via a reading unit for allocation to the outgoing bit stream.

A write-related pointer is given a value which corresponds to a transmission buffer bit position into which the writing unit writes, and a read-related pointer is given a value which corresponds to a transmission buffer bit position from which the reading unit reads.

The first transmission frequency or bit rate may differ from the second transmission frequency or bit rate, and consequently a checking and adjusting means which includes a proportional part, an integrating part and an adjusting part is adapted to check the bit distance between the write-related

pointer and the read-related pointer and, when necessary, to adjust the bit distance between the writing and the reading units.

The proportional part compares the difference between the value given to the write-related pointer and the value given to the read-related pointer with a first limit value, and the integrating part adds the deviation between said difference to an anticipated value, where the sum obtained is comparable with a second limit value.

The result of one of these comparisons is operative in initiating adjustment of the distance between the writing and the reading units through the medium of the adjusting part.

The proportional part and the integrating part operate with a specific clock frequency.

DESCRIPTION OF THE BACKGROUND ART

It has long been known to use a transmission buffer at the transition from a first transmission system using one certain type of transmission protocol to a second transmission system using another type of transmission protocol.

Different frequency tolerances in the transporting bit streams are specified in different transmission systems, and the different transmission systems also include mechanisms for handling these frequency tolerances. This means that the bit rate in the first transmission system can differ from the bit rate in the second transmission system.

It is also known that even when information is transmitted at a well-defined and stable bit rate, the bit rate may vary slightly when the signal is received and when transmitted over long distances, due to different kinds of distortion.

The fact that two different transmission systems can operate at different transmission speeds and that the first transmission speed or bit rate can vary slightly in time necessitates the inclusion of a transmission buffer in order to enable a well-defined and stable bit rate to be obtained in the second transmission system.

Information from the first transmission system is written into a transmission buffer by a writing unit and is read from the same buffer by a reading unit, to form standard data frames within the second transmission system.

It is also known to use two pointers, one representing the buffer position into which information shall be written and one representing the position from which information shall be read, and to detect or measure the distance between these positions so as to be able to adjust the speed of the reading unit and/or the writing unit and therewith prevent the reading unit catching up with the writing unit, or vice versa, and also prevent information being destroyed, for instance as a result of the writing unit writing over information that has not yet been read (read and write pointer overlap).

It is also desirable to prevent highly frequent disturbances in bit speed, jitter, and less frequent disturbances in bit speed, drift, present in the first transmission system from being transferred to the second transmission system.

The term "jitter" relates to deviations of the bit positions from their nominal positions in time at variations above 10 Hz, while with "drift" is meant deviations of the bit positions from their nominal positions in time at variations beneath 10 Hz.

In these contexts, it is also known to use an adjusting method which is referred to as stuffing in this document and which means that those data frames used in the second trans-

mission system are allocated so-called adjuster bits which can be filled or left empty, depending on whether the first rate is higher or lower than the bit rate that can be expected from the first transmission system.

Such deviation of the first bit rate from the expected bit rate will cause one pointer to come closer to the other pointer and in certain cases the pointers may even overlap and therewith destroy information.

In these contexts, stuffing is the most common method of enabling the bit distance of the writing and the reading units to be adjusted and therewith avoid the problem of overlapping pointers and compensating for jitter and drift respectively.

In these respects, it is also known to use so-called proportional adjustment involving continuous evaluation of the bit distance in the transmission buffer between the write-related pointer and the read-related pointer, and using stuffing to adjust the distance between the writing unit and the reading unit when the distance falls beneath a predetermined limit value.

This adjustment method may result in slightly uneven stuffing which, in turn, can result in jitter in the second transmission system. It is therefore desirable that stuffing is distributed as evenly as possible in time, to prevent jitter in the second transmission system.

It is also known to use so-called integrating adjustment, meaning that a mean or aggregate value of the bit distance in the transmission buffer between the write-related pointer and the read-related pointer is formed continuously over a predetermined time period, T, whereafter the mean value distance thus formed is used to obtain by integration a value that can be compared with an expected or anticipated distance. This

method enables trends occurring due to drift to be detected, and stuffing can be carried out before it is necessary to do so as a result of exceeding a limit in accordance with the proportional adjustment.

This adjustment provides more uniform stuffing and thereby enables jitter in the second transmission system to be avoided.

It is also known to use both proportional and integrating adjustment in parallel.

Examples of earlier known systems that use this type of checking and adjustment of a transmission buffer are disclosed in publications US-A-5,263,056, US-A-5,337,315, US-A-5,132,970, US-A-5,331,671 and WO-A1-94 00935.

A large number of logic circuits are required to form a mean value of the bit distance between the two pointers and to integrate/summate or add together several mean values, which in turn requires space, the application of error controls and possibly error corrections and high power inputs with subsequent necessary cooling of components.

Also known to the art are different transmission systems having different types of transmission protocols.

One such transmission protocol, which is characterized by high demands with respect to the time positions of the bit positions (jitter and drift), permits large quantities of data to be transmitted at high transmission speeds without the need of multiplexing and demultiplexing in transmission and reception respectively, and is designated SDH (Synchronous Digital Hierarchy).

An older transmission protocol with which multiplexing and demultiplexing is necessary in transmission and reception can

accept larger deviations in the time positions of the bit positions (jitter and drift), this protocol being designated PDH (Plesiosynchronous Digital Hierarchy).

In a transition from a PDH-domain to an SDH-domain, it is therefore very important that drift and jitter that may be present in the PDH-domain are not transferred to the SDH-domain. Consequently, it is known to use the aforedescribed transmission buffer and stuffing method at precisely such transitions.

It is also known to use stuffing in a node within a domain, in order to be able to handle frequency deviations between different node-clocks in the transmission system.

SUMMARY OF THE PRESENT INVENTION

TECHNICAL PROBLEMS

When considering the earlier standpoint of techniques as described in the aforegoing, it will be seen that in respect of a system which is intended to check and adjust a transmission buffer wherein a bit stream incoming to the buffer has a first transmission frequency or bit rate and wherein a bit stream outgoing from the buffer has a second transmission frequency or bit rate, wherein the information contained in each of the bits belonging to the incoming bit stream can be written into the buffer via a writing unit and the information contained in each of the bits written into the buffer can be read via a reading unit for allocation to the outgoing bit stream, wherein a write-related pointer is given a value that corresponds to a buffer bit position into which the writing unit writes and a read-related pointer is given a value which corresponds to a buffer bit position from which the reading unit reads, wherein the first transmission frequency or bit rate may differ from the second transmission frequency or bit rate, wherein a checking and adjusting means

that includes a proportional part, an integrating part and an adjusting part checks and adjusts the bit distance between the write-related pointer and the read-related pointer, wherein the proportional part compares a difference between the value given to the write-related pointer and the value given to the read-related pointer with a first limit value, wherein the integrating part adds the deviation between said difference to an anticipated value through the medium of an adder or a summating unit, wherein the sum obtained is comparable with a second limit value, and wherein the result of one of the comparisons made is operative in initiating an adjustment of said distance through the medium of the adjusting part, a technical problem resides in realizing how an integrating part can be obtained through the medium of relatively simple, power-lean but still highly effective circuitry.

Another technical problem is one of realizing the fact that an integrating adjustment can be achieved with a lower clock frequency than that necessary to achieve a proportional adjustment, and also to realize the possibilities afforded by this fact.

It will also be seen that a technical problem resides in realizing how jitter and drift damping in the incoming bit stream can be increased in relation to known techniques in a simple and cost-effective manner.

Another technical problem is one of realizing the possibilities that are created when the proportional part is allowed to operate at a first clock frequency and to allow the integrating part to operate at a second clock frequency which has a significantly lower value than the first clock frequency.

Still another technical problem is one of realizing the conditions required for the integrating part to be able to operate at a lower frequency than the proportional part.

Another technical problem is one of realizing the advantages that are afforded when the first clock frequency is comprised of a system-determined clock frequency, and those possibilities that are afforded when the second clock frequency is variable.

It will also be seen that a technical problem is one of realizing how the possibility of allowing the second clock frequency to be variable can be created.

It will also be seen that a further technical problem is one of realizing the value that shall be allocated to the second clock frequency in relation to the first clock frequency so as to thereby obtain a desired technical effect.

Another technical problem is one of realizing the conditions that are required for the proportional part to provide satisfactory adjustment of the reading unit and/or the writing unit in relation to drift and jitter and differences in bit rates between the first and the second bit rates.

Another technical problem is one of realizing the conditions that are required for the integrating part to provide satisfactory adjustment of the reading unit and/or the writing unit in relation to drift and jitter and differences in the bit rate between the first and the second bit rates.

It will also be seen that a further technical problem is one of realizing the advantages that are afforded when certain vital components within the proportional part and the integrating part can be common to both of said parts, and also the conditions necessary herefor.

A technical problem also resides in realizing the significance of allowing the incoming bit stream and the outgoing bit stream to derive from separate transmission protocols.

It will also be seen that a technical problem is one of realizing the significance of and the advantage afforded by allowing one transmission protocol to be comprised of a PDG-protocol and the other transmission protocol to be comprised of an SDH protocol.

A technical problem also resides in realizing the advantages that are afforded when the second transmission frequency or bit rate is system-determined and dependent on the SDH protocol.

Another technical problem will be seen to reside in realizing those advantages that are afforded when a first clock frequency is allotted the same frequency as the system-determined second transmission frequency or bit rate.

It will also be seen that a technical problem resides in realizing those advantages that are afforded when adjustment of the distance between the reading unit and the writing unit can be effected by so-called stuffing.

It will also be seen that a further technical problem is one of realizing those conditions that are necessary in providing necessary stuffing possibilities.

SOLUTION

With the intention of solving one or more of the aforesaid technical problems, the present invention takes as its starting point a system for checking and adjusting a transmission buffer, wherein a bit stream incoming to the transmission buffer has a first transmission frequency or bit rate, and wherein a bit stream outgoing from the transmission buffer has a second transmission frequency or bit rate.

According to known techniques, the information contained in each of the bits of the incoming bit stream can be written

into the transmission buffer via a writing unit, and the information contained in each of the bits written into the buffer can be read via a reading unit for allocation to the outgoing bit stream.

Further, a write-related pointer is given a value which corresponds to a bit position in the transmission buffer that the writing unit writes into, and a read-related pointer is given a value which corresponds to a bit position in the buffer from which the reading unit reads.

The first transmission frequency or bit rate can differ from the second transmission frequency or bit rate and a checking and adjusting means includes a proportional part, an integrating part and an adjusting part and checks and adjusts the bit distance between the writing unit and the reading unit so as to thereby avoid overlapping of the units and therewith prevent spreading of jitter and drift from the first transmission frequency to the second transmission frequency.

According to known techniques, the proportional part is adapted to compare a difference between the value given to the write-related pointer and the value given to the read-related pointer with a first limit value, and the integrating part adds the deviation between the difference to an expected value via a summating unit or adder and compares the sum obtained with a second limit value, wherein the result of one of these comparisons is intended to initiate adjustment of the bit distance between the reading unit and the writing unit through the medium of the adjusting part.

It is specifically proposed in accordance with the invention that the integrating part includes a down-sampling unit whereby the integrating part can operate with a clock frequency that is lower than the clock frequency at which the remainder of the system operates.

As a result, the proportional part operates with a first clock frequency, the integrating part operates with a second clock frequency, and the second clock frequency is given a lower value than the first clock frequency.

It is also proposed that the down-sampling unit is adjustable, therewith enabling the second clock frequency to be varied.

It is proposed that the second clock frequency is of the order of 500 to 1500, preferably about 1000, times lower than the first clock frequency.

With a first clock frequency in the region of 2 to 3 MHz, which is a typical clock frequency range in known techniques, a second clock frequency which is 1000 times lower than the first clock frequency will effectively smooth out frequency deviations that lie in the order of from 1 to 1.5 kHz according to the Nyquist criterion, which is the region in which much of the jitter and primarily the drift lies.

The proportional part can be built-up around a first subtraction unit which is adapted to detect a difference between the value given to the write-related pointer and the value given to the read-related pointer, and a first comparison unit which is adapted to compare the obtained difference with a first limit value.

The integrating part can be built-up around a second subtraction unit which is adapted to detect a difference between the value given to the write-related pointer and the value given to the read-related pointer, a third subtraction unit which is adapted to detect a deviation between the difference detected by the second subtraction unit and an expected or anticipated difference, a summating unit or adder which is adapted to summate a plurality of consecutive deviations detected by the third subtraction unit, a second comparison

unit which is intended to compare the obtained sum with a second limit value, and a zeroing unit which is adapted to set the summating unit or adder to zero upon initiation of an adjustment by the second comparison unit.

It is also conceivable to make the process more simple and more effective by mutually combining the first subtraction unit belonging to the proportional part and the second subtraction unit belonging to the integrating part in one common subtraction unit.

The system can also be used when the incoming bit stream derives from a first transmission protocol and the outgoing bit stream is allotted a second transmission protocol.

The invention also enables the first transmission protocol to be comprised of a PDH protocol and the second transmission protocol to be comprised of an SDH protocol.

In an SDH protocol, it is normal for the system-determined transmission frequency or bit rate to reach up to 2,304 MHz.

It is also proposed in accordance with the invention that, for the sake of simplicity, the first clock frequency coincides with the system-determined transmission frequency and is therefore also in the order of 2,304 MHz.

The adjusting part is adapted to adjust the distance between the writing unit and the reading unit by stuffing, in accordance with the result of one of the comparisons made in the proportional part and the integrating part respectively.

The outgoing bit stream is formed into standard data frames in accordance with the protocol used, and the stuffing is comprised in that at least two bits in each outgoing data frame constitute adjustment bits:

- where both adjustment bits are devoid of information when an adjustment is initiated because a comparison shows that the first transmission frequency or bit rate is lower than the second transmission frequency or bit rate,

- where both adjustment bits are allocated information when an adjustment is initiated because a comparison shows that the first transmission frequency or bit rate is higher than the second transmission frequency or bit rate, or

- where one adjustment bit is devoid of information and one adjustment bit is allocated information if no adjustment is initiated.

Each adjustment bit is allocated a check bit which is adapted to indicate whether an associated adjustment bit is filled or not.

ADVANTAGES

Those advantages that are primarily characteristic of a system according to the present invention reside in the creation of possibilities of checking and adjusting writing into and reading from a digital transmission buffer, wherein an initiated adjustment is able to smooth-out deviations in the time positions of the bit positions in relation to expected deviations, and wherein the adjustment is able to compensate for those differences in transmission frequency or bit rate that can exist in the transition from one transmission protocol to another, and specifically in the transition from one PDH-domain to an SDH-domain, to an extent required for the transmission of information within an SDH-domain. This is afforded by the present invention with fewer components and with more effective damping of occurrent jitter and drift than is possible when practicing known techniques.

The primary characteristic features of an inventive system are set forth in the characterizing clause of the following Claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

A system having features characteristic of the present invention will now be described in more detail by way of example and with reference to the accompanying drawings, in which

Figure 1 is a schematic and greatly simplified illustration of how the flow of information is able to pass from one domain to another;

Figure 2 is a block schematic illustrating a transmission buffer with associated checking and adjusting system;

Figure 3 illustrates the function of a circular transmission buffer;

Figure 4 illustrates cut-off frequencies and related damping or smoothing effects of parts in the system that are allocated different clock frequencies;

Figure 5 illustrates the function of an integrating part in two diagrams, diagram A and diagram B;

Figure 6 illustrates a proposed embodiment of a downsampling unit;

Figure 7 illustrates an alternative embodiment of parts of a checking and adjusting system;

Figure 8 illustrates the principle construction of a data

frame; and

Figure 9 illustrates an alternative embodiment having a plurality of parallel transmission buffers.

DESCRIPTION OF PROPOSED EMBODIMENTS

The present invention relates to a system which is intended to act as a buffer between two different types of transmission protocol or in a node between two transmission protocols of mutually the same type.

In this latter case, there is a need to dampen or smooth-out the occurrence of jitter and drift so as to prevent the same from being propagated and spread through the system, and to compensate for different clock frequencies of different node clocks. The performance requirement in this case is not as high as in the former case, but the present invention will nevertheless find use in the latter case since the invention provides both a high performance solution and a cost-effective solution.

The requirements in the former case are greater, because a considerable difference can exist between the transfer frequencies or bit rates in the two different transmission protocols. It may be so that one protocol is a PDH protocol, whereas the other protocol is an SDH protocol. In this case, extremely high demands are placed on the buffer acting between the two protocols, so as to be able to satisfy the high time-precision requirements relating to the SDH protocol.

Figure 1 is an extremely simplified illustration of how information departs from a transmitter A1 located in a first domain A, e.g. a PDH-domain, where a first transmission frequency A_f or bit rate is operative.

The receiver A'1 is located within a second domain A', e.g.

an SDH-domain, in which a second transmission frequency A'_f or bit rate is operative. In order to manage the conversions of data packet or data frames required in the transition from one domain to the other, there is provided a conversion arrangement B which acts as an interface between the two domains A, A'. Greatly simplified, this arrangement B includes a buffer B1, a receiving unit B2, a decoding unit B3, a coding unit B4 and a transmitter unit B5.

The receiving unit B2 receives digital information arriving in the form of standard data frames and at the first transmission frequency A_f or bit rate according to the protocol used in the first domain A. Each frame contains specific information related to the format of the frame within the protocol concerned, and address information denoting the receiver. The decoding unit B3 selects essential data bits that need to be forwarded in order for the information to reach the receiver A'1, while frame-specific data bits are scaled off.

The essential bits are written into the buffer B1, whereafter the bits are read from the buffer and forwarded to the coding unit B4. The information is here re-coded to form standard data frames according to the protocol used in the second domain A'.

The data frames are then sent into the second domain A' via the transmitting unit B5, at the second transmission frequency A'_f or bit rate and finally reach the receiver A'1.

The person skilled in this art will be aware that the information flow can pass in the other direction, although the following description refers to flow in only one direction for the sake of simplicity.

This technique is known to the art and because the present invention relates specifically to the function of the buffer

B1, remaining units in the conversion arrangement B will not be described here. Similarly, the specific construction of data frames or data cells in accordance with different protocol is also known to the art and consequently such construction will not be described in detail in this document.

Figure 2 illustrates a system adapted to check and adjust at least one buffer B1 according to Figure 1. Among other things, the buffer B1 includes a transmission buffer 1 where a bit stream 11 incoming to the transmission buffer has a first transmission frequency f_1 or bit rate and where a bit stream 12 outgoing from the buffer 1 has a second transmission frequency f_2 or bit rate.

The information contained in each of the bits of the incoming bit stream 11 can be written into the transmission buffer 1 through the medium of a writing unit 13, and the information contained in each of the bits written into the buffer 1 can be read via a reading unit 14 for allocation to the outgoing bit stream 12.

Figure 3 illustrates a transmission buffer 1 which may have the form of a circular FIFO (First In - First Out) buffer which, in the case of the described embodiment, is allocated 48 bits numbered from 0 to 47. A write-related pointer 15 is constantly allocated a value which corresponds to the bit position into which the write unit 13 writes, and a read-related pointer 16 is constantly allocated a value corresponding to the bit position from which the reading unit 14 reads.

Because the first transmission frequency f_1 or bit rate can differ temporarily from the second transmission frequency f_2 or bit rate due to jitter and drift, and also continuously due to the practical function within the conversion arrangement B, the buffer B1 also includes a checking and adjusting arrangement which checks the bit distance between the two

units 13, 14 and which can initiate adjustment of this distance, so as to prevent the reading unit 14 coming too close to the writing unit 13 or overlapping said unit, or vice versa.

The checking and adjusting arrangement includes a proportional part 2, an integrating part 3, and an adjusting part 4, and functions to check the bit distance between the write-related pointer 15 and the read-related pointer 16, so as to be able to adjust the bit distance between the writing unit and the reading unit 13, 14.

In the Figure 2 embodiment, the proportional part 2 includes a first subtraction unit 21 which is adapted to detect a difference between the value given to the write-related pointer 15 and the value given to the read-related pointer 16, and a first comparison unit 22 which is adapted to compare the obtained difference with a first limit value "a".

If this comparison shows that the bit distance between the two pointers 15, 16 is too small, the comparison unit 4 initiates adjustment of the distance between the units 13 and 14.

Figure 2 also shows that the integrating part 3 includes a second subtraction unit 31 which is adapted to detect a difference between the value given to the write-related pointer 14 and the value given to the read-related pointer 16, a third subtraction unit 32 which is adapted to detect a deviation between the difference detected by the second subtraction unit 31 and an expected or anticipated difference "b", a summating unit or adder 33 which is adapted to summate a plurality of consecutive deviations, a second comparison unit 34 which is adapted to compare the sum obtained with a second limit value "c", and a zeroing unit 35 which is adapted to set the summating unit 33 to zero upon adjustment initiated by the second comparison unit 34.

The integrating part 3 also includes a down-sampling unit 36 whereby the integrating part can operate with a clock frequency that is lower than the clock frequency at which the remainder of the system operates.

This means that the proportional part 2 operates at a first clock frequency, that the integrating part 3 operates at a second clock frequency, and that the second clock frequency is allocated a lower value than the first clock frequency.

This solution provides a relatively simple circuit construction (combinatorial logic and adders) of the integrating part 3 where no power-demanding, mean-value forming circuit that works at high frequencies is necessary.

Figure 4 shows that according to the Nyquist criterion a lower cut-off frequency of the integrating part will result in a higher damping or smoothing effect within the active frequency range, since the clock frequency can be compared in this case with a sampling frequency.

According to the Nyquist criterion, the cut-off frequency of the active range is corresponded by about half the sampling frequency (the clock frequency), which gives the integrating part 3 a cut-off frequency f_1 which is much lower than the cut-off frequency f_p of the proportional part 2. It is true that the active frequency regions will decrease markedly at a lower sampling frequency (clock frequency), but since the purpose of the damping of the integrating part is primarily to dampen or smooth out low frequency disturbances, this decrease constitutes no limitation to the function.

On the other hand, it is appropriate to allow the proportional part to operate at the same clock frequency as the system frequency used, so as to be able to still compensate for rapid variations in the difference between the two transmission frequencies f_1, f_2 or bit rates.

The writing unit 13 writes continuously at the speed at which data bits 11 arrive at the buffer. The reading unit 14 reads continuously at the speed required to form data frames within the second domain A'. However, there is room in the construction of the data frames within the second domain for given adjustment to the speed of the reading unit 14, either an increase or decrease in speed.

Figure 3 shows that the first limit value "a" towards which the proportional part 2 works is comprised of two margins, an overfill margin "a_1" and an underfill margin "a_2", which are intended to indicate the risk of an overfull or empty buffer.

In the illustrated case, the first limit value "a" has been chosen as ± six bits distributed uniformly around the value of the read-related pointer 16.

If the reading unit 14 comes within six bits of the writing unit 13, there is a danger that the buffer 1 will be emptied, meaning that it is necessary to reduce the reading speed to some extent, whereas if the writing unit 13 comes within six bits of the reading unit 14, there is a danger of the buffer becoming overfull, meaning that the reading speed must be increased to some extent.

Figure 3 also shows the so-called buffer depth B_d, which is corresponded by the number of bits that have been written into the buffer but are still unread, in other words the distance between the writing unit and the reading unit.

Figure 5 is intended to illustrate the function of the integrating part still further and to show what the second limit value "c" that the integrating part works towards is corresponded by.

Figure 5 shows two diagrams A and B. Diagram A is intended to show how the buffer depth varies with time. The time axis

solely shows the buffer depth when the integrating circuit receives a value, in other words when the second clock frequency is 1000 times lower than the first clock frequency, the diagram A solely shows the buffer depth at each thousandth bit, and hence the buffer depth can vary markedly between two consecutive time points. It should be mentioned, however, that the variations in Figure 5 are only simulated for the purpose of illustrating the principle of the integrating part 3.

Diagram A shows variations in the buffer depth in the absence of adjustment to the reading speed with filled bars, whereas corresponding variations with adjustment are shown by empty bars.

Similarly, diagram B shows with filled bars the value in the summating unit or adder 33 with neither adjustment nor zeroing of the summating unit, whereas empty bars show the value in the summating unit when the summating unit has been adjusted and zeroed at a chosen threshold value. The time points in diagram B are corresponded by the same time points in diagram A.

The summating unit 33 stores the deviation of the detected buffer depth B_d, which is the value arriving from the third subtraction unit 32, from a desired buffer depth. In diagram A, the desired buffer depth is 24 bits, which is normal in a practical application with an FIFO buffer that includes 48 bits.

Since the summating unit 33 summates consecutive deviations, with signs, diagram B will show for each time period, with signs, the combined area beneath the buffer depth curve according to diagram A from the latest zeroing of the summating unit 33 to the current time point. Thus, with a starting point from zeroing the summating unit at time point No. 0, the instantaneous value of the summating unit at time point

No. 10 will, according to diagram B, correspond to the area beneath the curve between time point No. 0 and time point No. 10 in accordance with diagram A.

The other limit value "c" is determined by a largest or smallest threshold value "c_1", "c_2" which for the purpose of illustration is shown in diagram B as ± 65 bits.

Diagram B shows that the summated value reaches the higher threshold value "c_1" at time point No. 13, therewith initiating adjustment of the distance between the reading unit and the writing unit, as shown at time point No. 14 in diagram A, and the summating unit 33 is zeroed by the zeroing unit 35, as shown at time point No. 14 in diagram B. Further adjustments take place at time points 25, 26; 31, 32 and 48, 49.

The diagrams show that in the case of slow variations, the integrating part initiates an adjustment before the buffer depth reaches the limit value "a", which in diagram A is corresponded by the buffer depth 6, "a_2" in Figure 3, and 42 bits respectively, "a_1" in Figure 3. The buffer depth is able to reach these limits in the case of rapid variations, however, wherewith one or more adjustments will be initiated by the proportional part.

Figure 6 shows that the down-sampling unit 36 may include a frequency divider 36a which divides the system frequency used, and, e.g., two AND gates 36b, 36b' which only pass through a value from the two pointers 15, 16 with the same frequency as the divided frequency f_{nd}. Those units that operate in the integrating part will then operate at the clock frequency f_{nd}.

The down-sampling unit may also be adjustable by using an adjustable frequency divider 36a where the frequency-division factor can be chosen arbitrarily. This enables the second clock frequency to be variable and set to a desired value.

A suitable frequency-division factor of the system frequency is to divide the frequency so that the second clock frequency will have a value in the order of 500 to 1500, preferably about 1000 times lower than the first clock frequency.

This frequency division enables the components used in the integrating part 3 to be comprised of simpler and less power-consuming components than in the case when the integrating part 3 operates at the same clock frequency as the remaining parts.

In order to obtain with known techniques a result that is comparable with the result that can be expected with an inventive solution, it would be necessary to form a mean or aggregate value continuously in the integrating part over the time T (1/used clock frequency) in real time, resulting in the requirement of highly complex logic to these ends. A down-sampled integrating part in accordance with the invention therefore greatly reduces the amount of complex logic and therewith also the power consumption.

It can be mentioned that theoretically the power saving is proportional to the frequency-division factor squared, meaning that a power saving in the order of one-million times can be expected with a frequency-division factor of 1000.

This power saving is obtained chiefly because the logic in the integrating part according to the present invention is clocked at a lower speed, the divided frequency, than the logic required for use in accordance with known techniques in forming a mean value and clocked by the system clock, which is normally the second transmission frequency.

With the intention of saving further components, Figure 7 illustrates an embodiment in which the first subtraction unit 21, belonging to the proportional part 2, and the second subtraction unit 31, belonging to the integrating part 3, are

comprised of one common subtraction unit 17. In addition to saving one subtraction unit, this also enables the two AND-gates 36b, 36b' in the down-sampling unit 36 to be replaced by one AND-gate 36b".

In the case of this embodiment, the incoming bit stream derives from a first transmission protocol and the outgoing bit stream is transferred to a second transmission protocol, where the first transmission protocol is a PDH-protocol and the second transmission protocol is an SDH-protocol.

A typical transmission frequency for the bit streams to and from a transmission buffer according to this embodiment is 2,304 MHz, which corresponds to a standard PCM-protocol (Pulse Code Modulated) with information-carrying bits (payload) and protocol specific bits (overhead).

The second transmission frequency f_2, or bit rate, is therewith system-determined to 2,304 MHz.

It is therefore simple to allocate the first clock frequency a value of 2,304 MHz, since this frequency constitutes the system frequency f_s and is already available in the system.

According to the proposed embodiment, the adjusting part is adapted to effect an adjustment by so-called stuffing depending on the result from one of the two comparison units 22, 34.

As a part of the structure used to form data frames within an SDH-protocol, there is room for so-called adjustment bits with associated check bits. Figure 8 illustrates, for instance, the construction of a data frame within an SDH-protocol designated TU12 (Tributary Unit 12).

In the TU12 frame structure, there are two bits which constitute so-called adjustment bits, S1 and S2.

When forming a data frame, the adjustment is made by

- leaving both adjustment bits S1, S2 devoid of information when an adjustment is initiated because a comparison unit 22, 34 shows that the first transmission frequency f_1 or bit rate is lower than the second transmission frequency f_2 or bit rate,

- allocating information to both adjustment bits S1, S2 when an adjustment is initiated because a comparison unit 22, 34 shows that the first transmission frequency f_1 or bit rate is higher than the second transmission frequency f_2 or bit rate, or

- by allocating information to one adjustment bit S1 and by leaving one adjustment bit S2 devoid of information when no adjustment is initiated.

Each adjustment S1, S2 has an associated check bit C1, C2 which is adapted to indicate whether an associated adjustment bit is filled or not.

Figure 8 also shows a number of other bits which are used to construct the data frame in accordance with current protocol. However, the present invention is not dependent on these bits and consequently their function will not be described in detail here.

In making an adjustment, the adjustment unit 4 commands the reading unit 14, via conductor 41, to read a further bit over and above the normal reading speed, or to stop and refrain from reading a bit, depending on the type of adjustment that is initiated. At the same time, the coding unit B4 receives, via conductor 42, information necessary for filling the adjustment bits S1, S2 and to allocate the correct values to the check bits C1, C2 in accordance with the adjustment carried out and in accordance with the current protocol.

The second clock frequency is chosen so that a comparison will be made in the integrating part 3 once for each data frame formed in the second domain A'. The buffer depth is checked and the necessary adjustment evaluated in conjunction with writing-in the bits S1 and S2.

This enables the reading speed of the reading unit 14 to be adjusted by reading an extra bit and therewith increasing the reading speed at certain times, and to read one bit fewer and therewith reduce the reading speed at other times, all in accordance with existing requirements.

Applications are found, e.g., in byte-locked mapping where the information is handled in bytes, groups of n number of bits, where n is normally eight, and where parallel data processing is used. An inventive system can also be used in such an application, as shown in Figure 9.

Where n number of transmission buffers 1_1, 1_2 ... 1_n act in parallel and where the writing units and reading units included also act in parallel, it is sufficient to check solely one of the parallel-acting transmission buffers 1_1 included even though an adjustment initiated by the check must be carried out in parallel on all parallel-acting transmission buffers 1_1, 1_2 ... 1_n.

It will be understood that the invention is not restricted to the aforedescribed and illustrated embodiment and that modifications can be made within the scope of the inventive concept as illustrated in the following Claims.

CLAIMS

1. A system for checking and adjusting at least one transmission buffer, wherein a bit stream incoming to the transmission buffer has a first transmission frequency or bit rate, wherein a bit stream outgoing from the transmission buffer has a second transmission frequency or bit rate, wherein the information allocated to each of the bits of the incoming bit stream can be written into the transmission buffer through the medium of a writing unit and the information allocated to each of the bits written into the transmission buffer can be read through the medium of a reading unit and allocated to the outgoing bit stream, wherein a write-related pointer is given a value which corresponds to a bit position in the transmission buffer into which the writing unit writes, and a read-related pointer is allocated a value which corresponds to a bit position in the transmission buffer from which the reading unit reads, wherein said first transmission frequency or bit rate may differ from said second transmission frequency or bit rate, wherein a checking and adjustment means comprising a proportional part, an integrating part and an adjusting part functions to check the bit distance between the write-related pointer and the read-related pointer and, when necessary, adjust the bit distance between said writing unit and said reading unit, wherein the proportional part compares a difference between the value given to the write-related pointer and the value given to the read-related pointer with a first limit value, wherein the integrating part adds the deviation between said difference to an expected value with the aid of a summating unit, wherein an obtained sum is comparable with a second limit value, wherein the result of one of said comparisons is operable in initiating an adjustment of said distance with the aid of said adjusting part, and wherein the proportional part operates at a first clock frequency, c h a r a c t e r i z e d in that the integrating part includes a down-sampling unit; in that the integrating part operates at a second clock

frequency; and in that said second clock frequency is given a lower value than the first clock frequency.

2. A system according to Claim 1, c h a r a c t e r i z e d in that the first clock frequency is a system-determined clock frequency; in that the down-sampling unit is adjustable; and in that the second clock frequency is thereby variable.

3. A system according to Claim 1 or 2, c h a r a c t e r i z e d in that the second clock frequency is in the order of 500 to 1500, preferably about 1000, times lower than the first clock frequency.

4. A system according to Claim 1, c h a r a c t e r i z e d in that the proportional part includes a first subtraction unit which is adapted to detect a difference between the value given to the write-related pointer and the value given to the read-related pointer, and a first comparison unit which is adapted to compare the difference obtained with a first limit value.

5. A system according to Claim 1 or 4, c h a r a c t e r i z e d in that the integrating part includes a second subtraction unit which is adapted to detect a difference between the value given to the write-related pointer and the value given to the read-related pointer, a third subtraction unit which is adapted to detect a deviation between the difference detected by the second subtraction unit and an expected difference, a summating unit which is adapted to summate a plurality of consecutive deviations detected by said third subtraction unit, a second comparison unit which is adapted to compare the sum obtained with a second limit value, and a zeroing unit which is adapted to zero the summating unit in the case of an adjustment initiated by said second comparison unit.

6. A system according to Claim 4 or 5, c h a r a c t e r i z e d in that the first subtraction unit belonging to the proportional part, and the second subtraction unit belonging to the integrating part are comprised of a common subtraction unit.

7. A system according to Claim 1, c h a r a c t e r i z e d in that the incoming bit stream derives from a first transmission protocol; and in that the outgoing bit stream is converted in accordance with a second transmission protocol.

8. A system according to Claim 7, c h a r a c t e r i z e d in that the first transmission protocol is a PDH-protocol.

9. A system according to Claim 7, c h a r a c t e r i z e d in that the second transmission protocol is an SDH-protocol.

10. A system according to Claim 1, c h a r a c t e r i z e d in that the second transmission frequency or bit rate is system-determined; and in that said frequency or bit rate is between 2 MHz and 3 MHz, preferably 2,304 MHz.

11. A system according to Claim 1, c h a r a c t e r i z e d in that the first clock frequency is of the order of 2 MHz to 3 MHz, preferably about 2,304 MHz.

12. A system according to Claim 1, c h a r a c t e r i z e d in that the adjusting part is adapted to effect adjustment by stuffing, depending on the result of one of said comparisons.

13. A system according to Claim 12, c h a r a c t e r i z e d in that the outgoing bit stream is formed into standard data frames; in that said stuffing is comprised of at least two bits in each outgoing data frame constituting

adjustment bits; and in that

- both adjustment bits are left devoid of information when an adjustment is initiated because a comparison shows that said first transmission frequency or bit rate is lower than said second transmission frequency or bit rate,

- both adjustment bits are allocated information when an adjustment is initiated because a comparison shows that said first transmission frequency or bit rate is higher than said second transmission frequency or bit rate, or

- an adjustment bit is left devoid of information and an adjustment bit is allocated information when no adjustment is initiated;

and in that each adjustment is allocated a check bit which is adapted to indicate whether an associated adjustment bit is filled or not.

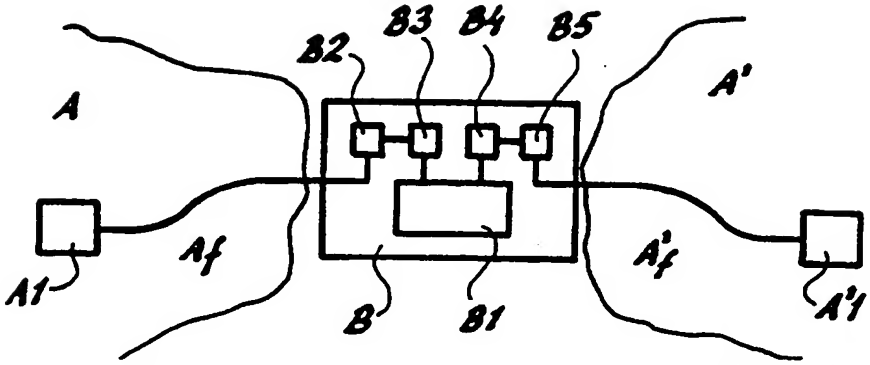

B2
B3
B4
B5
A
A'
A1
Af
A'f
A'1
B
B1

Fig. 1.

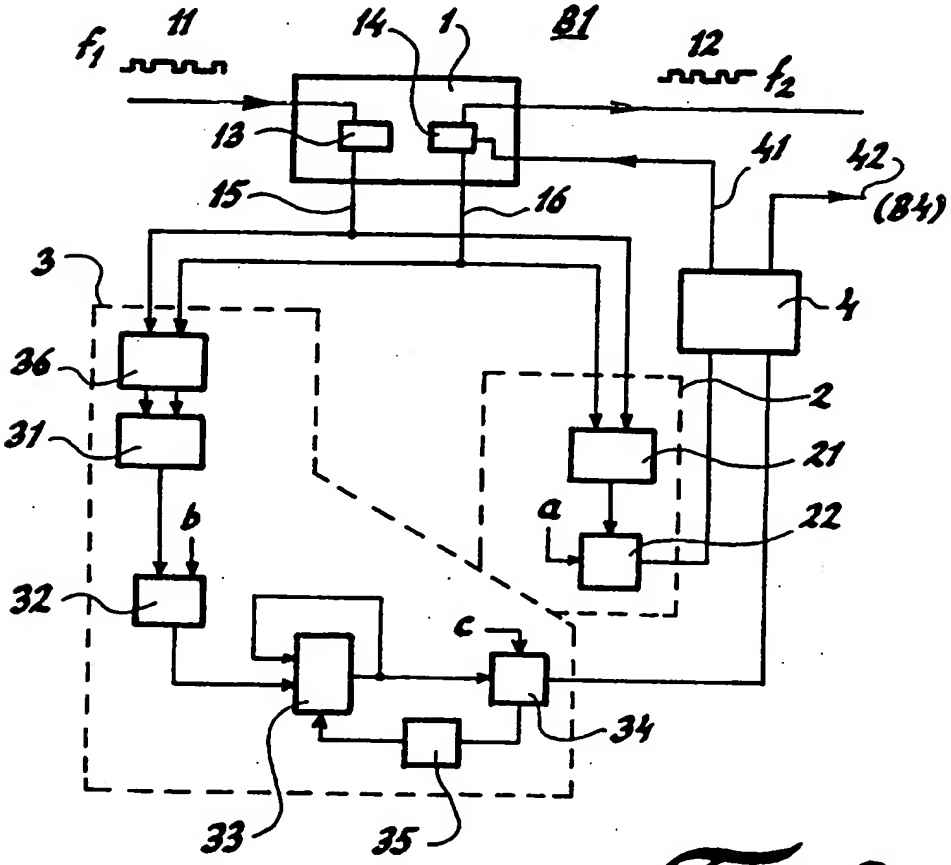

f1
11
14
1
B1
12
f2
13
41
42
(84)
15
16
3
4
36
2
31
21
a
22
b
32
c
34
33
35

Fig. 2.

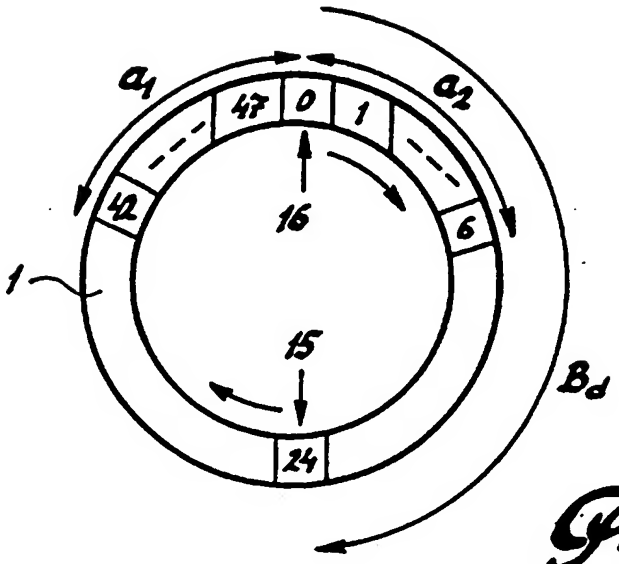


Fig. 3.

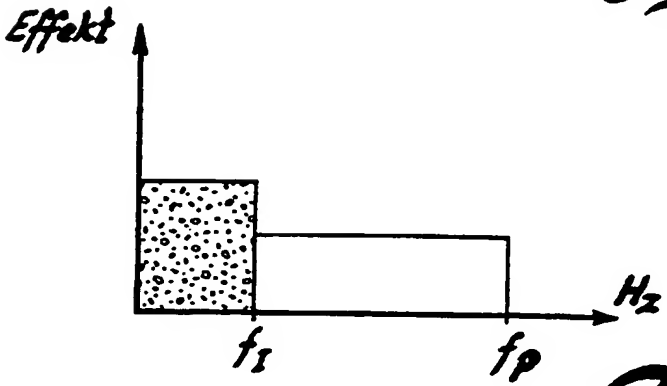


Fig. 4.

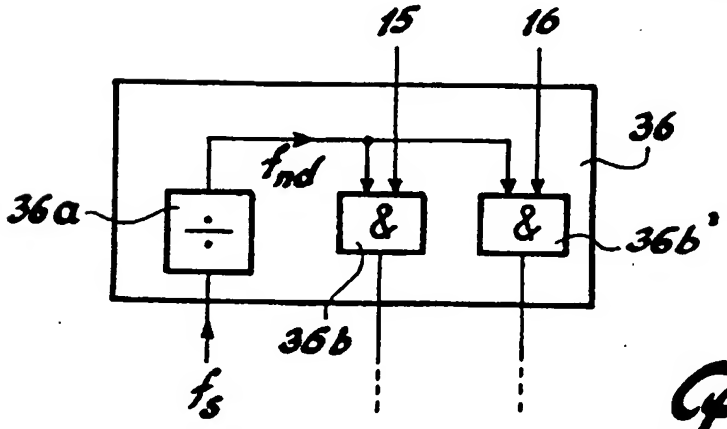


Fig. 6.

Diagram A

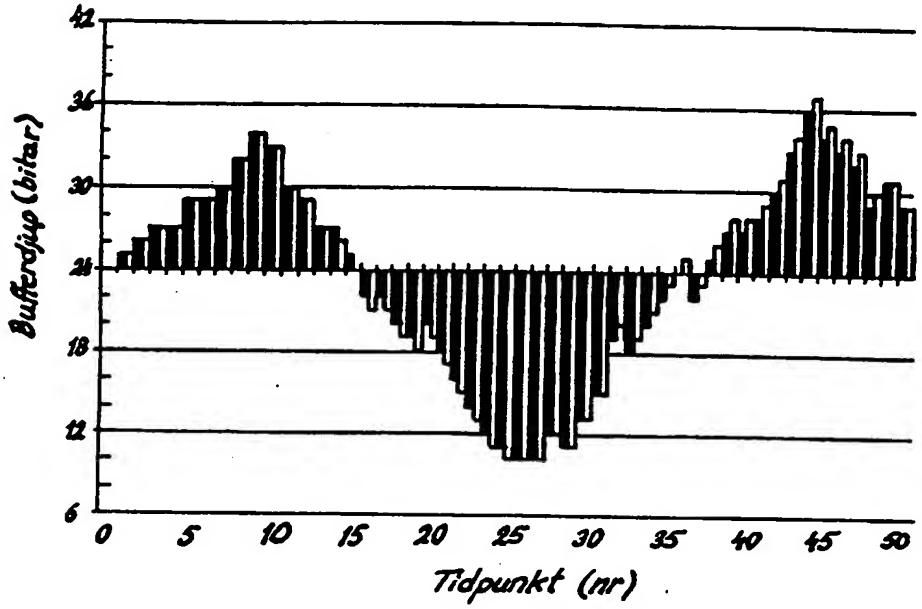


Diagram B

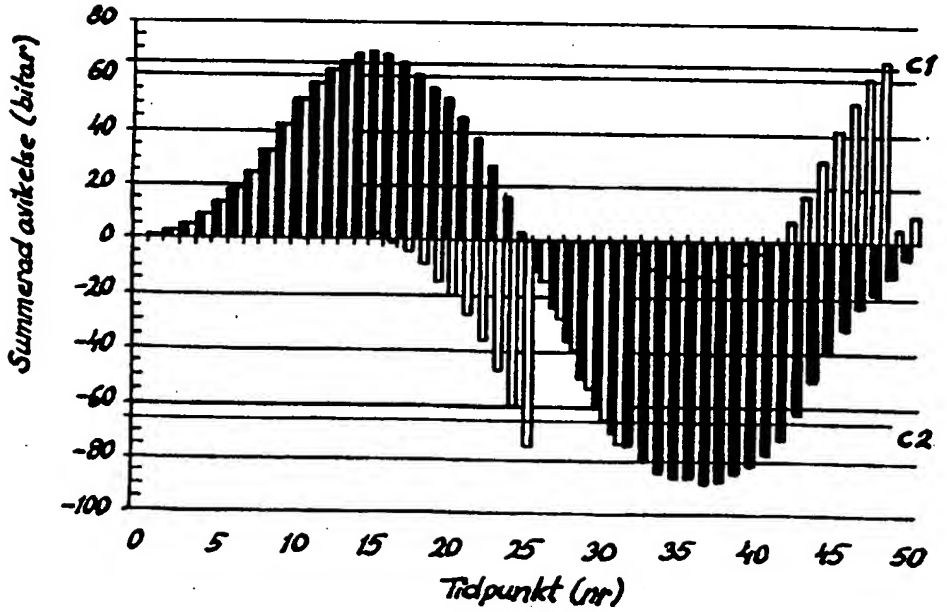


Fig. 5.

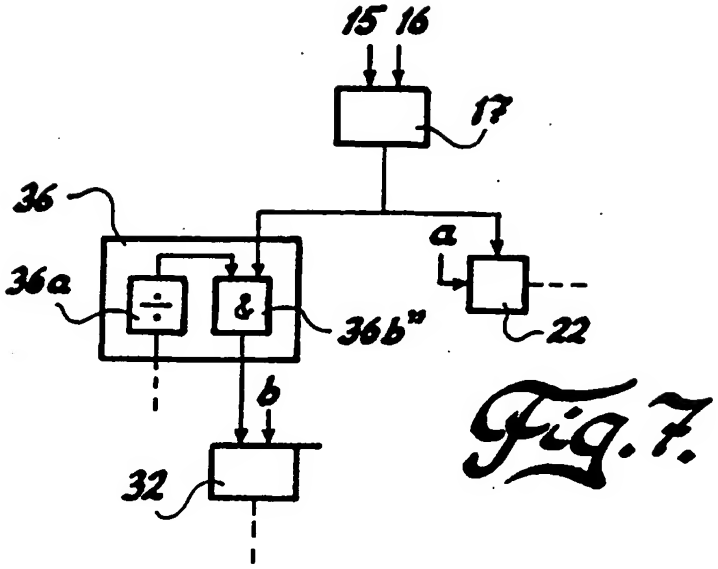


Fig. 7.

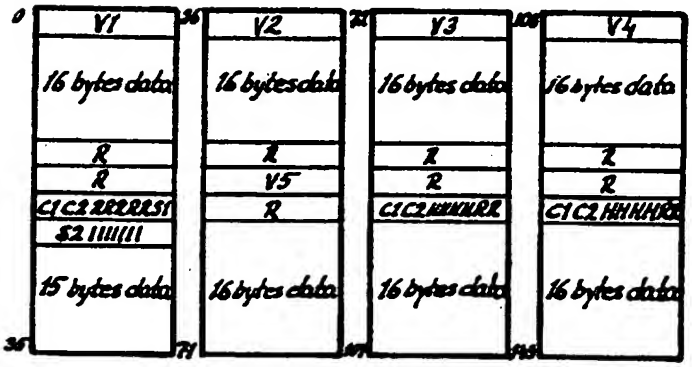


Fig. 8.

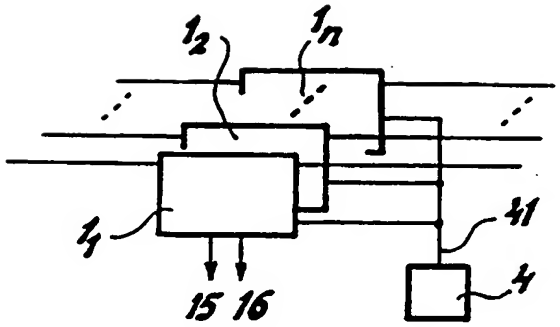


Fig. 9.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 96/01415

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04J 3/07, H04L 25/02, G06F 5/06
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04J, H04L, G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0475498 A2 (N.V. PHILIPS GLOEILAMPENFABRIEKEN), 18 March 1992 (18.03.92), column 3, line 51 - column 4, line 43, abstract --	1-13
A	EP 0572366 A1 (TELEFONAKTIEBOLAGET LM ERICSSON), 1 December 1993 (01.12.93), column 2, line 13 - column 4, line 29, abstract --	1-13
A	EP 0491054 A1 (FUJITSU LIMITED), 24 June 1992 (24.06.92), abstract --	1-13
A	WO 9422251 A1 (NOKIA TELECOMMUNICATIONS OY), 29 Sept 1994 (29.09.94), abstract --	1-13

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"B" erlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 January 1997	10 -02- 1997
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Mikael Sollerhed Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 96/01415

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 9318595 A1 (TRANSWITCH CORPORATION), 16 Sept 1993 (16.09.93), abstract --	1-13

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/SE 96/01415

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A2- 0475498	18/03/92	SE-T3- 0475498	
		AU-B- 653742	13/10/94
		AU-A- 8353291	12/03/92
		DE-A- 4027968	05/03/92
		DE-D- 59107198	00/00/00
		JP-A- 4227142	17/08/92
		US-A- 5331671	19/07/94
EP-A1- 0572366	01/12/93	AU-B- 664087	02/11/95
		AU-B- 666005	25/01/96
		AU-A- 3879293	02/12/93
		AU-A- 3879593	02/12/93
		EP-A- 0572367	01/12/93
		SE-B,C- 470392	07/02/94
		SE-A- 9201672	28/11/93
		SE-B,C- 470472	09/05/94
		SE-A- 9202774	26/03/94
EP-A1- 0491054	24/06/92	AU-B- 636050	08/04/93
		AU-A- 8189191	04/02/92
		JP-A- 4068625	04/03/92
		US-A- 5367545	22/11/94
		WO-A- 9201343	23/01/92
WO-A1- 9422251	29/09/94	AU-A- 6209694	11/10/94
		EP-A- 0689745	03/01/96
		FI-B,C- 93287	30/11/94
		FI-A- 931166	17/09/94
		JP-T- 8508146	27/08/96
WO-A1- 9318595	16/09/93	CA-A- 2130473	16/09/93
		IL-A- 104990	18/06/96
		IL-D- 113710	00/00/00
		JP-T- 7506944	27/07/95
		US-A- 5257261	26/10/93
		US-A- 5331641	19/07/94